

HI1176

October 25, 2005

8-Bit, 20 MSPS, Flash A/D Converter

### **Features**

- Resolution ±0.5 LSB (DNL) . . . . . . . . . . 8-Bit
- Maximum Sampling Frequency . . . . . . . . . 20 MSPS
- Low Power Consumption at 20 MSPS (Typ) (Reference Current Excluded) ......60mW
- Built-In Sync Clamp Function
- Built-In Monostable Multivibrator for Clamp Pulse Generation
- **Built-In Sync Pulse Polarity Selection Function**
- Clamp Pulse Direct Input Possible
- Built-In Clamp ON/OFF Function
- Built-In Reference Voltage Self Bias Circuit
- Input CMOS Compatible
- **Three-State TTL Compatible Output**
- Single +5V Power Supply
- Low Input Capacitance (Typ) . . . . . . . . . . . . 11pF
- Direct Replacement for the Sony CXD1176

### Description

The HI1176 is an 8-bit, CMOS analog-to-digital converter for video use that features a sync clamp function. The adoption of a 2-step parallel method realizes low power consumption and a maximum conversion speed of 20 MSPS. For higher sampling rates, refer to the pin-for-pin compatible HI1179 data sheet, document number 3666.

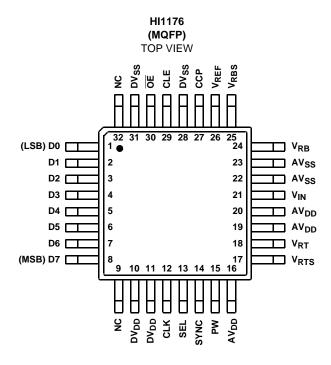
### **Applications**

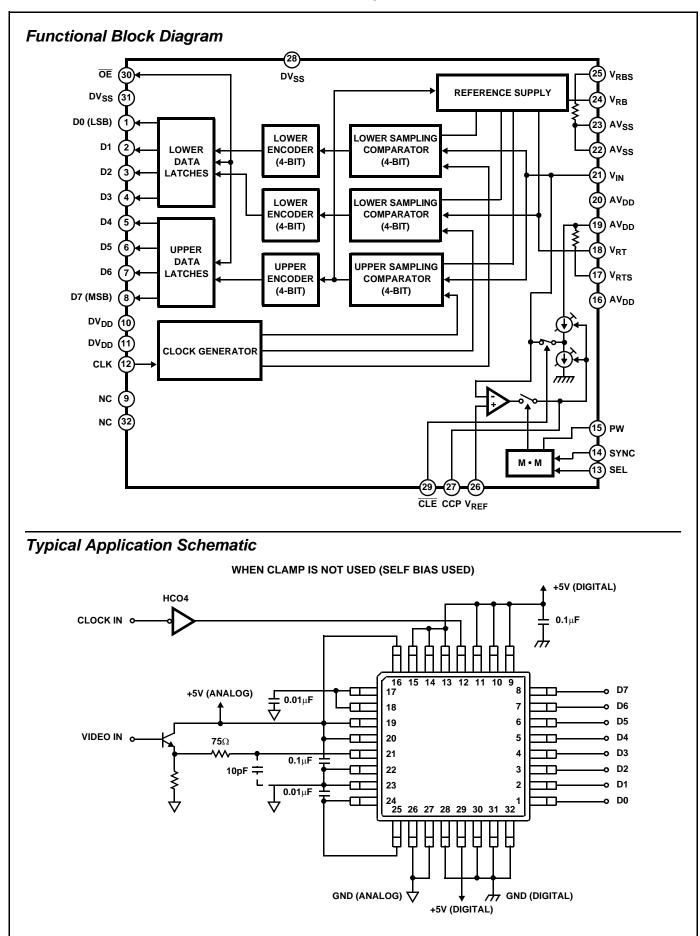
- · Video Digitizing
- Image Scanners
- Low Cost High Speed Data Acquisition Systems
- Multimedia

### Ordering Information

PART NUMBER	TEMP. RANGE ( <sup>O</sup> C)	PACKAGE	PKG. NO.
HI1176JCQ	-40 to 85	32 Ld MQFP	Q32.7x7-S
HI1176-EV	25	Evaluation Boar	d

### **Pinout**





### **Absolute Maximum Ratings**

# 

### Operating Conditions (Note 1)

Operating Conditions (Note 1)
Temperature Range, T <sub>A</sub> 40°C to 85°C
Supply Voltage
AV <sub>DD</sub> , AV <sub>SS</sub> , DV <sub>DD</sub> , DV <sub>SS</sub> +4.75V to +5.25V
DGND-AGND
Reference Input Voltage
V <sub>RB</sub> 0V and Above
V <sub>RT</sub> 2.8V and Below
Analog Input Voltage, V <sub>IN</sub> V <sub>RB</sub> to V <sub>RT</sub> (1.8V <sub>P-P</sub> to AV <sub>DD</sub> )
Clock Pulse Width
t <sub>PW1</sub>
t <sub>PW0</sub>

### **Thermal Information**

MQFP Package	Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ (oC/W)
Maximum Junction Temperature	MQFP Package	122
Maximum Lead Temperature (Soldering 10s)	Maximum Junction Temperature	150 <sup>o</sup> C
, ,	Maximum Storage Temperature Range65	5 <sup>o</sup> C to 150 <sup>o</sup> C
(Lead Tips Only)	Maximum Lead Temperature (Soldering 10s)	300°C
( )	(Lead Tips Only)	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE

1.  $\theta_{\mbox{\scriptsize JA}}$  is measured with the component mounted on an evaluation PC board in free air.

**Electrical Specifications**  $f_C = 20 \text{ MSPS}, V_{DD} = +5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25^{\circ}C \text{ (Note 1)}$ 

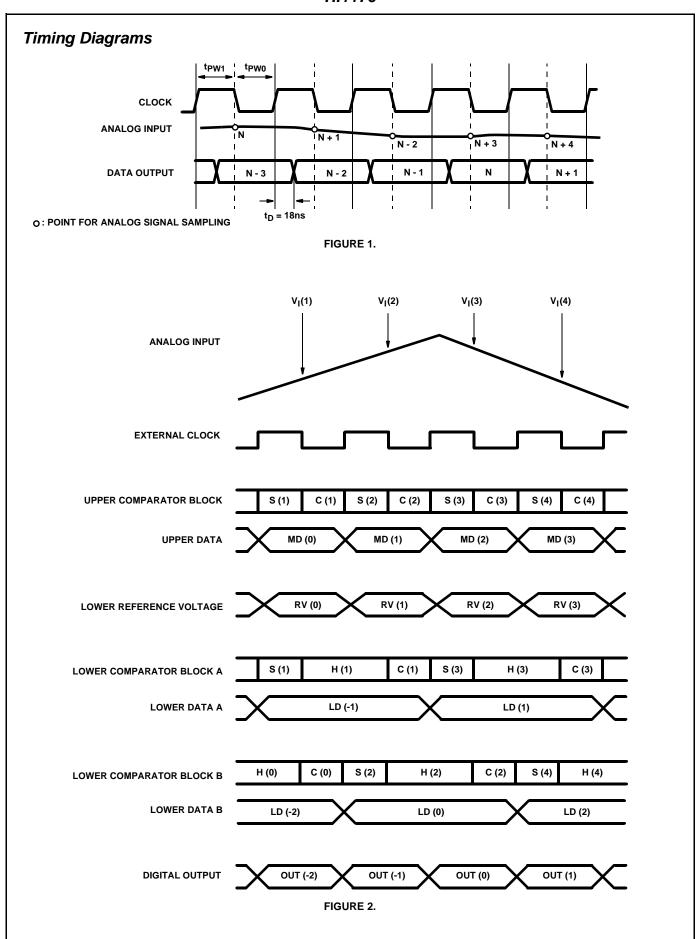
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Offset Voltage					
E <sub>OT</sub>		-60	-40	-20	mV
E <sub>OB</sub>		+20	+40	+60	mV
Integral Non-Linearity, INL	$f_C = 20 \text{ MSPS}, V_{IN} = 0.5V \text{ to } 2.5V$	-	±0.5	±1.3	LSB
Differential Non-Linearity, DNL	f <sub>C</sub> = 20 MSPS, V <sub>IN</sub> = 0.5V to 2.5V	-	±0.3	±0.5	LSB
DYNAMIC CHARACTERISTICS			•		•
Signal to Noise Ratio, SINAD	f <sub>S</sub> = 20MHz, f <sub>IN</sub> = 1MHz	-	46	-	dB
RMS Signal Signal-To-Noise + Distortion Ratio, SINAD	f <sub>S</sub> = 20MHz, f <sub>IN</sub> = 3.58MHz	-	46	-	dB
Maximum Conversion Speed, f <sub>C</sub>	$V_{IN} = 0.5V$ to 2.5V, $f_{IN} = 1kHz$ Ramp	20	35	-	MSPS
Minimum Conversion Speed		-	-	0.5	MSPS
Differential Gain Error, DG	NTSC 40 IRE Mod Ramp, f <sub>C</sub> = 14.3 MSPS	-	1.0	-	%
Differential Phase Error, DP		-	0.5	-	Degree
Aperture Jitter, t <sub>AJ</sub>		-	30	-	ps
Sampling Delay, t <sub>DS</sub>		-	4	-	ns
ANALOG INPUTS	L	1	1	1	1
Analog Input Bandwidth (-1dB), BW		-	18	-	MHz
Analog Input Capacitance, C <sub>IN</sub>	V <sub>IN</sub> = 1.5V + 0.07V <sub>RMS</sub>	-	11	-	pF

 $\textbf{Electrical Specifications} \quad \text{$f_C = 20$ MSPS, $V_{DD} = +5V$, $V_{RB} = 0.5V$, $V_{RT} = 2.5V$, $T_A = 25^{\circ}C$ (Note 1) } \quad \textbf{(Continued)}$ 

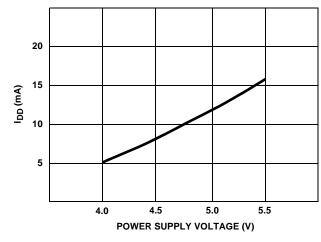
PARAMETER	TEST CONDI	TEST CONDITIONS		TYP	MAX	UNIT
REFERENCE INPUT				•		
Reference Pin Current, I <sub>REF</sub>			4.5	6.6	8.7	mA
Reference Resistance (V <sub>RT</sub> to V <sub>RB</sub> ), R <sub>REF</sub>			230	300	450	Ω
INTERNAL VOLTAGE REFERENCES					I	
Self Bias						
$V_{RB}$	Short V <sub>RB</sub> and V <sub>RBS</sub> , Short	V <sub>RT</sub> and V <sub>RTS</sub>	0.48	0.52	0.56	V
$V_{RT} - V_{RB}$			1.96	2.08	2.22	V
DIGITAL INPUTS						
Digital Input Voltage						
VIH			4.0	-	-	V
$V_{IL}$			-	-	1.0	V
Digital Input Current						
liH	$V_{DD} = Max$	$V_{IH} = V_{DD}$	-	-	5	μΑ
I <sub>IL</sub>		V <sub>IL</sub> = 0V	-	-	5	μА
DIGITAL OUTPUTS	<del>-</del>			_		
Digital Output Current						
ГОН	$\overline{OE} = V_{SS}, V_{DD} = Min$	$V_{OH} = V_{DD} - 0.5V$	-1.1	-	-	mA
I <sub>OL</sub>		V <sub>OL</sub> = 0.4V	3.7	-	-	mA
Digital Output Current						
OZH	$\overline{OE} = V_{DD}, V_{DD} = Max$	$V_{OH} = V_{DD}$	-	-	16	μΑ
l <sub>OZL</sub>		V <sub>OL</sub> = 0V	-	-	16	μА
TIMING CHARACTERISTICS	_			•	T	T
Output Data Delay, t <sub>DL</sub>			-	18	30	ns
POWER SUPPLY CHARACTERISTIC						
Supply Current, I <sub>DD</sub>	f <sub>C</sub> = 20 MSPS, NTSC Ramp	Wave Input	-	12	18	mA
CLAMP CHARACTERISTICS						
Clamp Offset Voltage, E <sub>OC</sub>	V <sub>IN</sub> = DC, PWS = 3μs	V <sub>REF</sub> = 0.5V	0	+20	+40	mV
		V <sub>REF</sub> = 2.5V	-50	-30	-10	mV
Clamp Pulse Width (Sync Pin Input), t <sub>CPW</sub>	$C = 100pF, R = 130k\Omega$ on Pi	n 15	1.75	2.75	3.75	μS
Clamp Pulse Delay, t <sub>CPD</sub>			-	25	-	ns

### NOTE:

<sup>1.</sup> Electrical specifications guaranteed only under the stated operating conditions.



### **Typical Performance Curves**



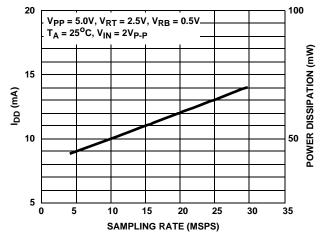


FIGURE 3. SUPPLY CURRENT vs SUPPLY VOLTAGE

FIGURE 4. SUPPLY CURRENT AND POWER vs SAMPLING

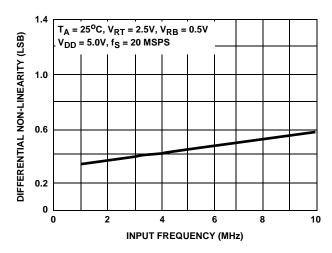


FIGURE 5. DIFFERENTIAL NON-LINEARITY vs INPUT FREQUENCY

### Pin Descriptions

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1-8	D0 to D7		D0 (LSB) to D7 (MSB) Output.
10, 11	$DV_DD$		Digital +5V.

# Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
12	CLK	12 DV <sub>DD</sub>	Clock Input.
13	SEL	13 DV <sub>DD</sub>	When SEL is low, the falling edge of Pin 14 (sync) triggers the monostable.  When SEL is high, the rising edge of Pin 14 (sync) triggers the monostable.
14	SYNC	14 DV <sub>DD</sub>	Trigger pulse input to the monostable multivibrator. Trigger polarity can be controlled by Pin 13 (SEL).
15	PW	15 DV <sub>SS</sub>	When a clamp pulse is generated by the monostable, the pulse width is determined by the external R and C.  When the clamp pulse is directly input, it is input to Pin 15 (PW).
16, 19, 20	AV <sub>DD</sub>		Analog +5V.
17	V <sub>RTS</sub>	Ŷ <sup>AV</sup> DD	When shorted with V <sub>RT</sub> , generates approx. +2.6V.
18	V <sub>RT</sub>	φ AV <sub>DD</sub>	Reference Voltage (Top).
24	V <sub>RB</sub>	18 24 AV <sub>SS</sub>	Reference Voltage (Bottom).

# Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
21	VIN	21 AV <sub>SS</sub>	Analog Input.
22, 23	AV <sub>SS</sub>		Analog Ground.
25	V <sub>RBS</sub>	AV <sub>SS</sub>	When shorted with V <sub>RB</sub> , generates approx. +0.5V
26	V <sub>REF</sub>	26 AV <sub>SS</sub>	Clamp Reference Voltage Input.
27	ССР	27 AV <sub>DD</sub>	Integrates the voltage for clamp control.
28, 31	DV <sub>SS</sub>		Digital GND.
29	CLE	29 CLAMP PULSE	When $\overline{\text{CLE}}$ is low, clamp function is activated. When $\overline{\text{CLE}}$ is high, clamp function is OFF and onl the usual A/D converter function is active. By connecting $\overline{\text{CLE}}$ pin to DV $_{DD}$ via a severa hundred $\Omega$ resistance, the clamp pulse can be tested.
30	ŌĒ	30 DV <sub>DD</sub>	When $\overline{OE}$ is low, data is valid.  When $\overline{OE}$ is high, D0 to D7 pins are hig impedance.

TABLE 1. A/D OUTPUT CODE

INPUT SIGNAL	DIGITAL OUTPUT CODE								
VOLTAGE	STEP	MSB							LSB
$V_{RT}$	255	1	1	1	1	1	1	1	1
	•					•			
•	•					•			
•	•					•			
•	128	1	0	0	0	0	0	0	0
•	127	0	1	1	1	1	1	1	1
•	•					•			
•	•					•			
•	•					•			
$V_{RB}$	0	0	0	0	0	0	0	0	0

### **Detailed Description**

The HI1176 is a 2-step A/D converter featuring a 4-bit upper comparator group and two lower comparator groups of 4 bits each. The reference voltage can obtained from the onboard bias generator or be supplied externally. This IC uses an offset canceling type comparator that operates synchronously with an external clock. The operating modes of the part are input sampling/autozero (S), hold (H), and compare (C).

The operation of the part is illustrated in Figure 2. A reference voltage that is between V<sub>RT</sub>-V<sub>RB</sub> is constantly applied to the upper 4-bit comparator group. V<sub>I</sub>(1) is sampled with the falling edge of the first clock by the upper comparator block. The lower block A also samples V<sub>I</sub>(1) on the same edge. The upper comparator block finalizes comparison data MD(1) with the rising edge of the first clock. Simultaneously the reference supply generates a reference voltage RV(1) that corresponds to the upper results and applies it to the lower comparator block A. The lower comparator block finalizes comparison data LD(1) with the rising edge of the second clock. MD(1) and LD(1) are combined and output as OUT(1) with the rising edge of the third clock. There is a 2.5 cycle clock delay from the analog input sampling point to the corresponding digital output data. Notice how the lower comparator blocks A and B alternate generating the lower data in order to increase the overall A/D sampling rate.

### Power, Grounding, and Decoupling

To reduce noise effects, separate the analog and digital grounds.

Bypass both the digital and analog  $V_{DD}$  pins to their respective grounds with a ceramic  $0.1\mu F$  capacitor close to the pin.

### **Analog Input**

The input capacitance is small when compared with other flash type A/D converters. However, it is necessary to drive the input with an amplifier with sufficient bandwidth and drive capability. In order to prevent parasitic oscillation, it may be necessary to insert a resistor between the output of the amplifier and the A/D input.

#### Reference Input

The range of the A/D is set by the voltage between  $V_{RT}$  and  $V_{RB}$ . The internal bias generator will set  $V_{RTS}$  to 2.5V and  $V_{RBS}$  to 0.5V. These can be used as the part reference by shorting  $V_{RT}$  and  $V_{RTS}$  and  $V_{RBS}$ . The analog input range of the A/D will now be from 0.5V to 2.5V. If a  $V_{RB}$  below +0.5V is used the linearity of the part will be degraded.

Bypass  $V_{\mbox{\scriptsize RT}}$  and  $V_{\mbox{\scriptsize RB}}$  to analog ground with a  $0.1\mu\mbox{\scriptsize F}$  capacitor.

### **Clamp Operation**

The HI1176 provides a clamp option that allows the user to clamp a portion of the analog input to a voltage set by the V<sub>REF</sub> pin. The clamp function is enabled by bringing CLE low. An internal monostable multivibrator is provided that can be used to generate the clamp pulses. The monostable pulse width is determined by the external R and C connected to the PW pin. The trigger to the monostable is applied on the SYNC pin. The edge that triggers the monostable is determined by the SEL pin. When SEL is low the falling edge will trigger the monostable and when SEL is high the rising edge will trigger the monostable. Figure 6 shows the HI1176 configured for this mode of operation. The clamp pulse is latched by the ADC sampling clock. This is not necessary to the operation of the clamp function but if this is not done then a slight beat might be generated as vertical sag according to the relation between the sampling frequency and the clamp frequency.

The HI1176 can also be configured to operate with an external clamp pulse. In this case a negative going pulse is input to the PW pin.  $V_{\mbox{\footnotesize{IN}}}$  will now be clamped during the low period of the clamp pulse to the voltage on the  $V_{\mbox{\footnotesize{REF}}}$  pin. Figure 7 shows the HI1176 configured for this mode of operation.

Figure 1 illustrates the operation of HI1176 when the clamp function is not used.

# **Typical Application Circuits**

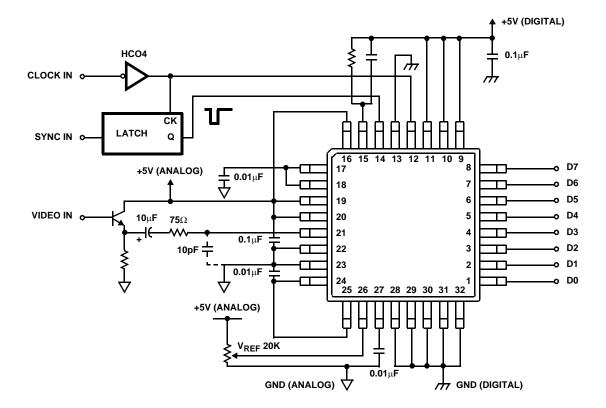


FIGURE 6. PEDESTAL CLAMP IS EXECUTED BY SYNC PULSE (SELF BIAS USED)

# Typical Application Circuits (Continued)

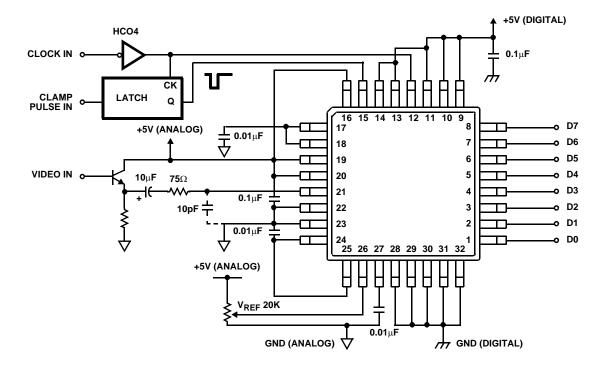


FIGURE 7. CLAMP PULSE IS DIRECTLY INPUT (SELF BIAS USED)

### **Test Circuits**

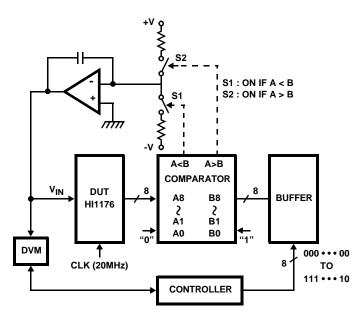


FIGURE 8. INTEGRAL AND DIFFERENTIAL NON-LINEARITY ERROR AND OFFSET VOLTAGE TEST CIRCUIT

### **Test Circuits**

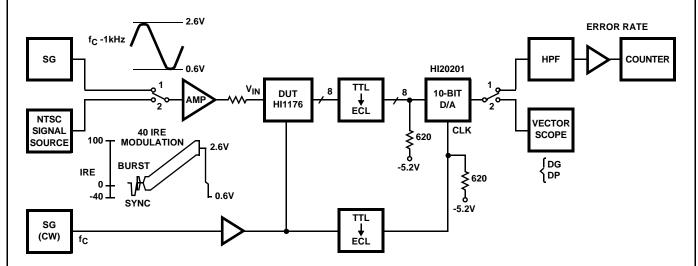


FIGURE 9. MAXIMUM OPERATIONAL SPEED AND DIFFERENTIAL GAIN AND PHASE ERROR TEST CIRCUIT

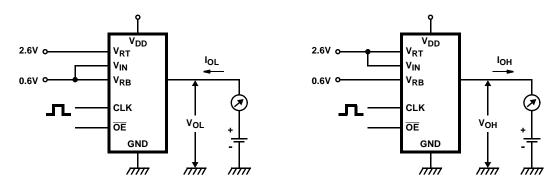


FIGURE 10. DIGITAL OUTPUT CURRENT TEST CIRCUIT

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